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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/717,495 | 11/20/2000 | Michael A. Fischer | 213.302 | 8490 |

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| EXAMINER | |
|---|---|
| CHANDRASEKHAR, PRANAV | |
| **ART UNIT** | **PAPER NUMBER** |
| 2115 | 9 |

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/717,495 | FISCHER, MICHAEL A. | |
| | Examiner | Art Unit | |
| | Pranav Chandrasekhar | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01/07/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 24,25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein [US Pat No. 5,666,522] in view of Takeda [US Pat No. 5,319,771].

2. As per claim 24, Klein teaches

executing instructions at a rate equal to that of a frequency of a function clock signal [col. 4 lines 16-18]; and

decreasing the frequency of function clock signal on the basis of decoded instructions [47 Fig 6;col. 6 lines 38-50].

Klein does not explicitly teach sending and receiving serial input/output data under the control of decoded instructions at a rate equal to the frequency of a source clock signal.

Takeda teaches decoding state discrimination signals of the CPU to determine the frequency of the clock signal (that dictates execution of commands). Furthermore, for commands that relate to sending input/output data, the decode logic causes the decrease of the frequency of the clock to that of a source clock on the basis of state discrimination signals [col. 9 lines 19-47].

Takeda does not explicitly teach sending and receiving serial input/output data.

It would have been obvious to one skilled in the art to combine the teachings of Klein and Takeda to use a decode logic to determine the type of operation denoted by the instruction and accordingly control the frequency of the clock signal and further decrease the frequency of the function clock signal to that of a source clock signal for sending and receiving serial input/output data to avoid using an additional explicit instruction for the sole purpose of decreasing clock frequency and hence accommodating the longer execution time associated with input/output data operations. Furthermore, it would be obvious to extend the concept of a decreased clock frequency for input/output data operations to serial input/output data operations.

3. As per claim 25, Klein and Takeda do not explicitly teach the sending and receiving of a single bit as a result of decoding an instruction.

It would have been obvious to one skilled in the art to modify the teachings of Klein and Takeda to send and receive one bit as a result of decoding a specific instruction.

4. As per claim 27, Klein and Takeda do not explicitly teach decoding and executing a delay instruction, thereby causing a delay in the further execution of instructions for a number of cycles of the function clock signal specified in a count field, wherein said delay is achieved by asserting an alternate inhibit signal so as to temporarily reduce the frequency of the function clock signal.

It would have been obvious to modify the teachings of Klein and Takeda to incorporate a count field in the instruction to delay the further execution of instructions for a certain number of cycles of the function clock signal by asserting an alternate inhibit signal so as to temporarily reduce the frequency of the function clock signal to facilitate additional clock cycles with reduced frequency for the execution of specific instructions.

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klein [US Pat No. 5,666,522] in view of Takeda [US Pat No. 5,319,771] as applied to claim 24 above, and further in view of Touriguian et al [US Pat No. 5,832,257].

Klein and Takeda do not explicitly teach repeating the execution of an instruction over a predetermined number of bit cells at rate equal to that of a source clock.

Touriguian teaches a repeat counter connected to the instruction decoder whereby a number is loaded into the repeat counter indicating how many times the execution of an instruction must be repeated. [col. 17 lines 16-30].

It would have been obvious to one skilled in the art to combine the teachings of Klein and Takeda with those of Touriguian to load a repeat counter with a number such that the execution of the instruction is repeated over a predetermined number of bit cells and thus avoiding the decoding of a separate consecutive instruction to repeat the same operation as that of the said instruction. Furthermore, it would have been obvious to enable the repeated instruction execution to take place at a source clock frequency.

6. Claims 17-19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein [US Pat No. 5,666,522] in view of Takeda [US Pat No. 5,319,771] and further in view of Kiuchi et al [US Pat No. 4,958,276].

7. As per claim 17, Klein teaches

an instruction decoder for controlling the operation of an apparatus based on the decoding of a specific instruction [ 47 Fig 6; col. 6 lines 38-50]; and

a function clock generator for generating a function clock signal that governs the rate of instruction execution within said apparatus, and wherein the frequency of the said function clock signal is decreased to equal frequency of a source clock signal upon the decoding of said specific instruction [40 Fig 6; col. 4 lines 16-18; col. 6 lines 38-50]

Klein does not explicitly teach

circuitry for sending and receiving serial input/output data at a rate equal to that of a source clock signal;

a memory for storing instructions connected to said instruction decoder;

a program counter connected to function clock generator, said memory and to said instruction decoder;

Takeda teaches circuitry for sending and receiving input/output data and the concept of decoding state discrimination signals of the CPU to determine the frequency of the clock signal (that dictates execution of commands). Furthermore, for commands that relate to sending input/output data, the decode logic causes the decrease of the frequency of the clock to that of a source clock on the basis of state discrimination signals [col. 9 lines 19-47].

Takeda does not explicitly teach

a memory for storing instructions connected to said instruction decoder;

a program counter connected to function clock generator, said memory and to said instruction decoder;and

sending and receiving serial input/output data.

Kiuchi teaches

memory for storing instructions [104 and 103 Fig 1; col. 2 lines 60-65]; and

a program counter connected to function clock generator, memory and detection circuit wherein the clock frequency of the clock to the program counter is determined by the detection circuit on the basis of the location of the instruction in memory [105 Fig 1; col. 8 lines 30-48]

Kiuchi does not teach sending and receiving serial input/output data.

It would have been obvious to one skilled in the art to combine teachings of Klein, Takeda and Kiuchi to use a decode logic to determine the type of operation denoted by the instruction and accordingly control the frequency of the clock signal and further decrease the frequency of the function clock signal to that of a source clock signal for sending and receiving serial input/output data to avoid using an additional explicit instruction for the sole purpose of decreasing clock frequency and accommodating the longer execution time associated with input/output data operations. Furthermore, it would have been obvious to extend the concept of a decreased clock frequency for input/output data operations to serial input/output data operations. In addition, the use of a program counter and a memory for storing instruction is

advantageous in that it accounts for the use of predefined instructions stored in memory that are sequentially fetched on the basis of the address denoted by the program counter. The frequency associated with the execution of instructions would denote the time at which the address of the program counter is incremented to fetch each subsequent instruction.

8. As per claims 18 and 19, Klein, Takeda and Kiuchi do not explicitly teach sending and receiving one bit of serial data on the basis of decoding a specific instruction.

It would have been obvious to one skilled in the art to modify the teachings of Klein, Takeda and Kiuchi to send and receive one bit of serial data on the basis of decoding a specific instruction.

9. As per claim 23, Klein, Takeda and Kiuchi do not explicitly teach the specific instruction being encoded using no more than eight bits.

It would have been obvious to one skilled in the art to modify the teachings of Klein, Takeda and Kiuchi to use an instruction that is encoded with no more than eight bits.

10. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein [US Pat No. 5,666,522] and Takeda [US Pat No. 5,319,771] in view of Kiuchi et al [US Pat No. 4,958,276] as applied to claim 17 above, and further in view of Touriguian et al [US Pat No. 5,832,257].

Klein,Takeda and Kiuchi do not explicitly teach the use of a repeat counter for receiving a count value indicating the number of times that the execution of a specific instruction is to be repeated.

Touriguian teaches a repeat counter connected to the instruction decoder whereby a number is loaded into the repeat counter indicating how many times the execution of an instruction must be repeated. [col. 17 lines 16-30].

It would have been obvious to one skilled in the art to combine the teachings of Klein, Takeda and Kiuchi with those of Touriguian to load a repeat counter with a number such that the execution of the instruction is repeated a predetermined number of times as dictated by a received count value and thus avoiding the decoding of a separate consecutive instruction to repeat the same operation as that of the said instruction.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
March 19,2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100